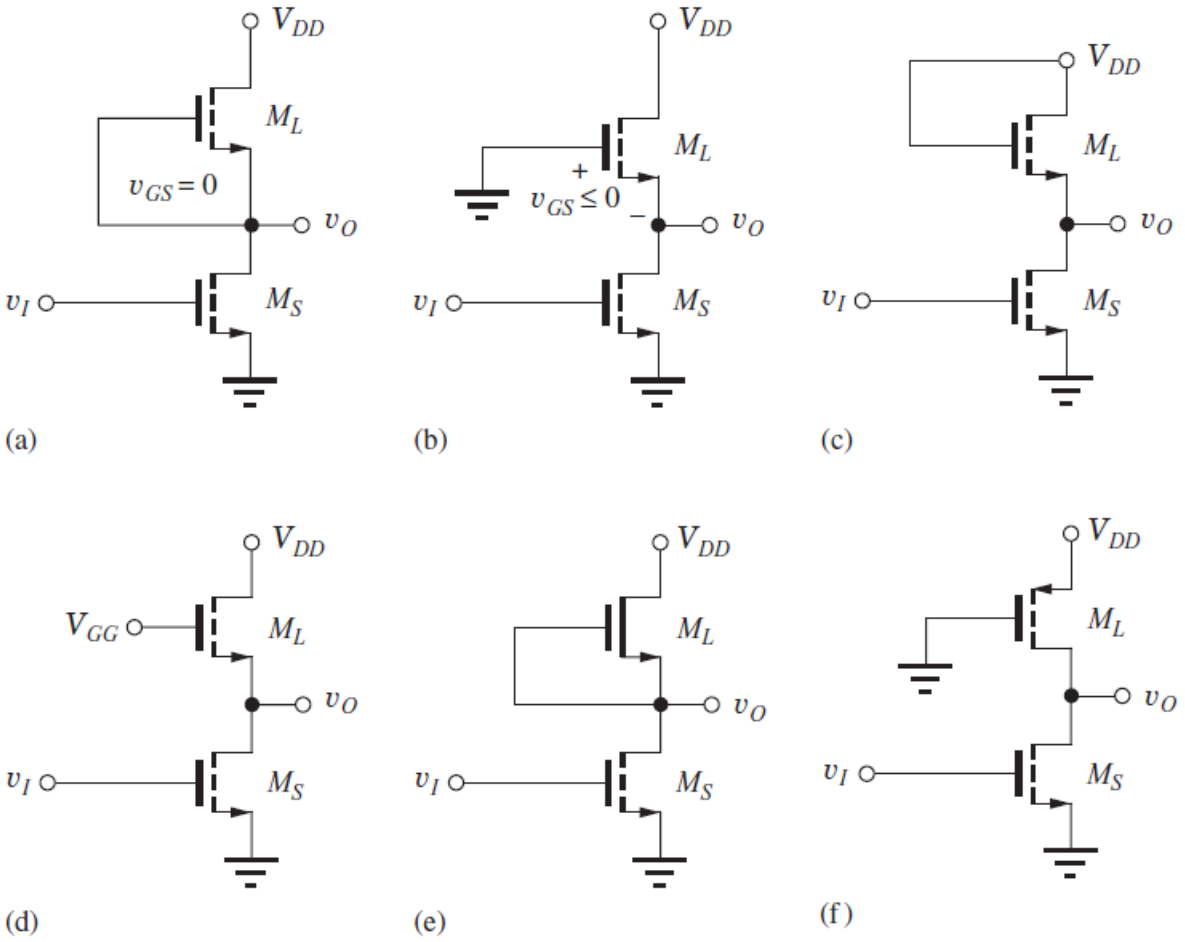
Announcements

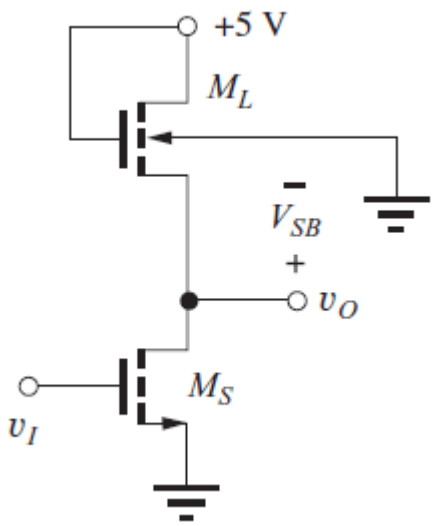
- Exam 2 in class on Monday 5/19
  - Chapters 4.1-4.6, 4.9-4.10, 6.1-6.2, and 6.4-6.8
  - MOSFET device behavior
  - MOSFETs in circuits and NMOS inverters/logic
  - HWs 4-6

Transistor alternatives to load resistor

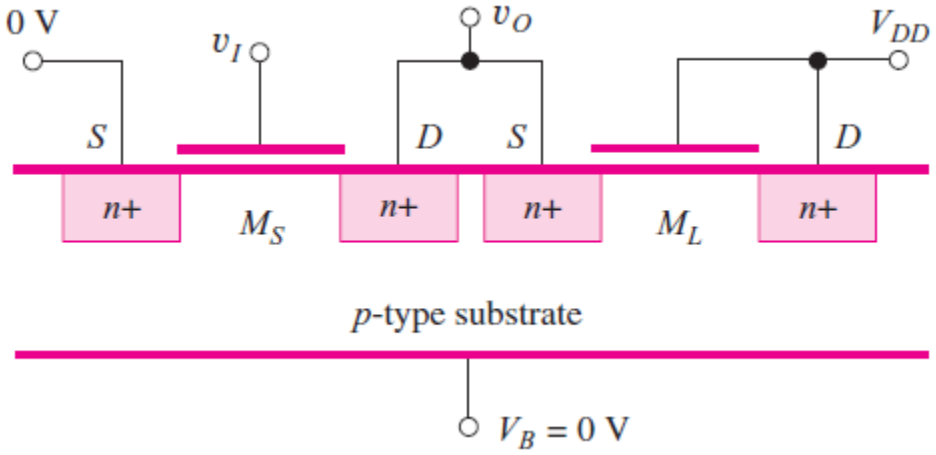


- (a,b) X
- c: saturated load √
- d: linear load √
- e: depletion-mode load √
- f: pseudo NMOS √

NMOS saturated load inverter



$v_{GS} = v_{DS}, V_{TN} > 0$
$\Rightarrow v_{GS} - V_{TN} < v_{DS}$
$\Rightarrow$ Always in saturation

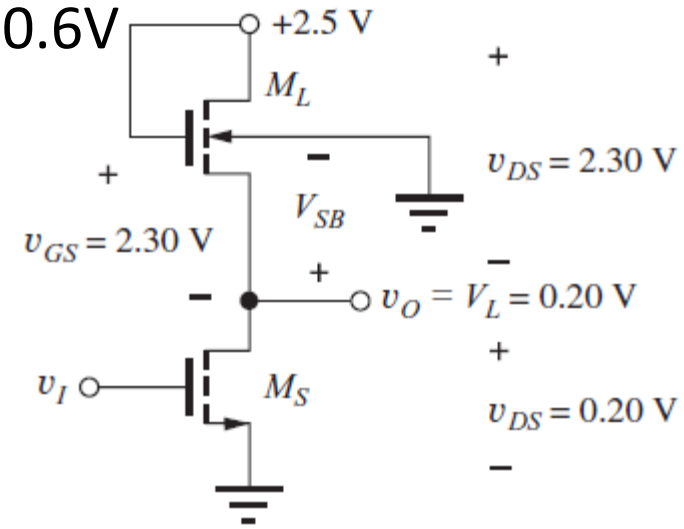


- Common substrate for load and switching device
- Body terminal connected to ground
  - $v_{SB} = 0$ for M_S
  - $v_{SB} \neq 0$ for M_L ! In fact, $v_{SB} = v_O$

Design of $\left(\frac{W}{L}\right)_L$ (Load transistor)

K_n'=100μA/V²

V_{TO}=0.6V



$v_I = V_H, v_O = V_L$

Current determined by permissible power dissipation of the NMOS, $\boldsymbol{P = V_{DD} I_{DD}}$

$v_I = V_H$, M_S triode, M_L saturation

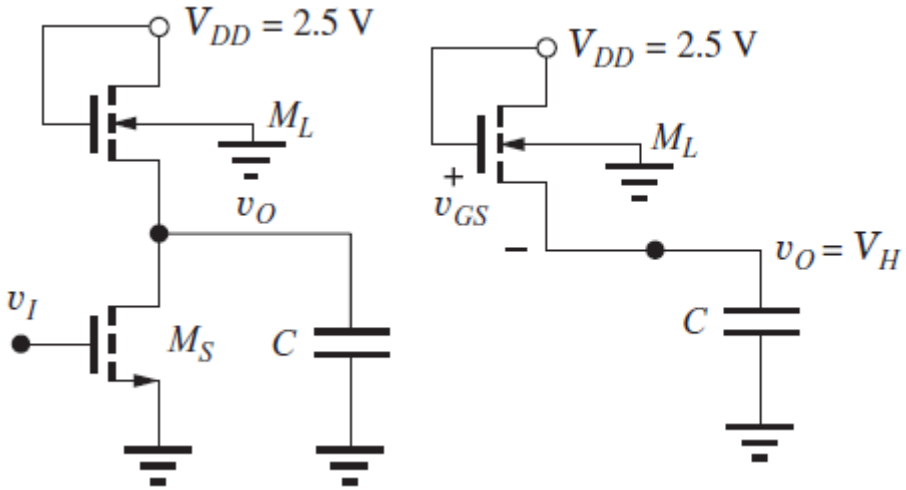
- Use the same conditions as before: $I_{DD} = 80\ \mu\text{A}, V_{DD} = 2.5\ \text{V}, V_L = 0.20\ \text{V}$
- Saturation region equation for M_L:

$$i_D = K_n' \left(\frac{W}{L}\right)_L (v_{GS} - V_{TNL})^2$$

- $v_{GS} = V_{DD} - V_L = 2.3\ \text{V}$
- Body effect for M_L:
- $V_{TNL} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$
- $v_{SB} = V_L = 0.2\text{V}, 2\phi_F = 0.6\text{V}, V_{TO} = 0.6\text{V}, \gamma = 0.5\sqrt{\text{V}} \Rightarrow V_{TNL} = 0.66\text{V}$
- $\left(\frac{W}{L}\right)_L = \frac{2i_D}{K_n'(v_{GS} - V_{TNL})^2} = \frac{1}{1.68}$

Calculation of V_H

$v_I = V_L, v_O = V_H, M_S$ Cutoff



Imagine a capacitive load attached in parallel with M_S

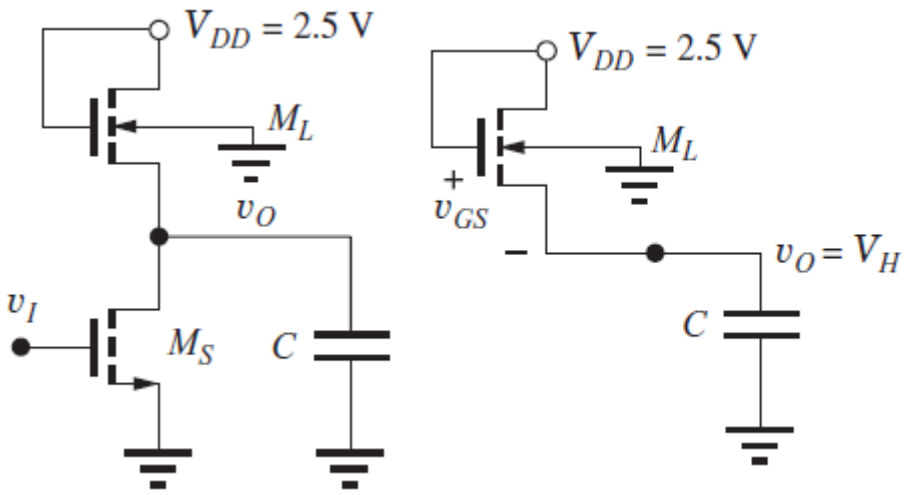
- When $v_I = V_L$, M_S is cutoff, M_L saturated (on) and charging the capacitor.
- As capacitor gets charged,
  - v_O increases
  - v_{GS} for M_L decreases
- Charging stops when M_L turns off ($v_{GS} = V_{TNL}$), and

$$V_H = V_{DD} - v_{GS} = V_{DD} - V_{TNL}$$

- V_H reaches maximum of one V_T below V_{DD}
- Substantial degradation in V_H for the saturated load inverter!

Calculation of V_H

$v_I = V_L, v_O = V_H, M_S$ Cutoff



Imagine a capacitive load attached in parallel with M_S

- $V_H = V_{DD} - V_{TNL}$
- Without Body effect,
  $V_H = 2.5\text{ V} - 0.6\text{ V} = 1.9\text{ V}$
- Body effect makes the situation even worse!
- Use $v_{SB} = V_H$ and solve

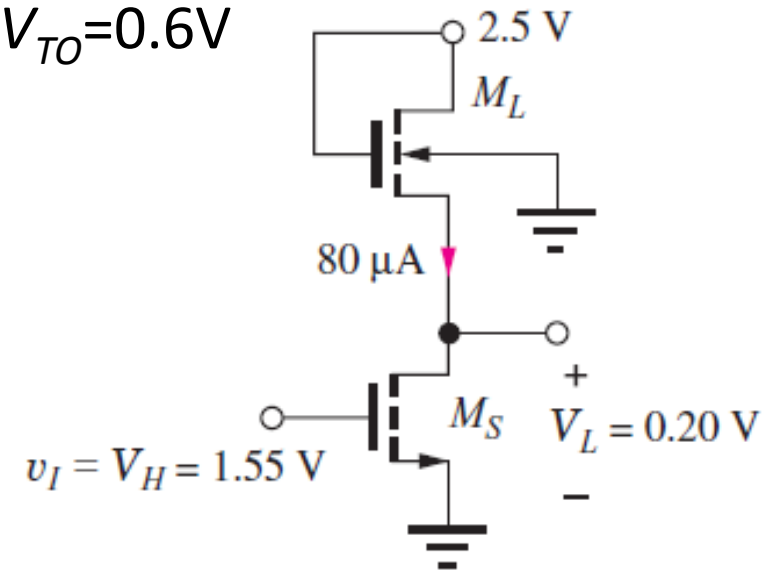
$$V_{DD} - V_H = V_{TO} + \gamma\left(\sqrt{V_H + 2\phi_F} - \sqrt{2\phi_F}\right)$$

- We get

$$V_H = 1.55\text{ V}$$

Design of $\left(\frac{W}{L}\right)_S$ (Switching transistor)

K_n'=100μA/V²
V_{TO}=0.6V

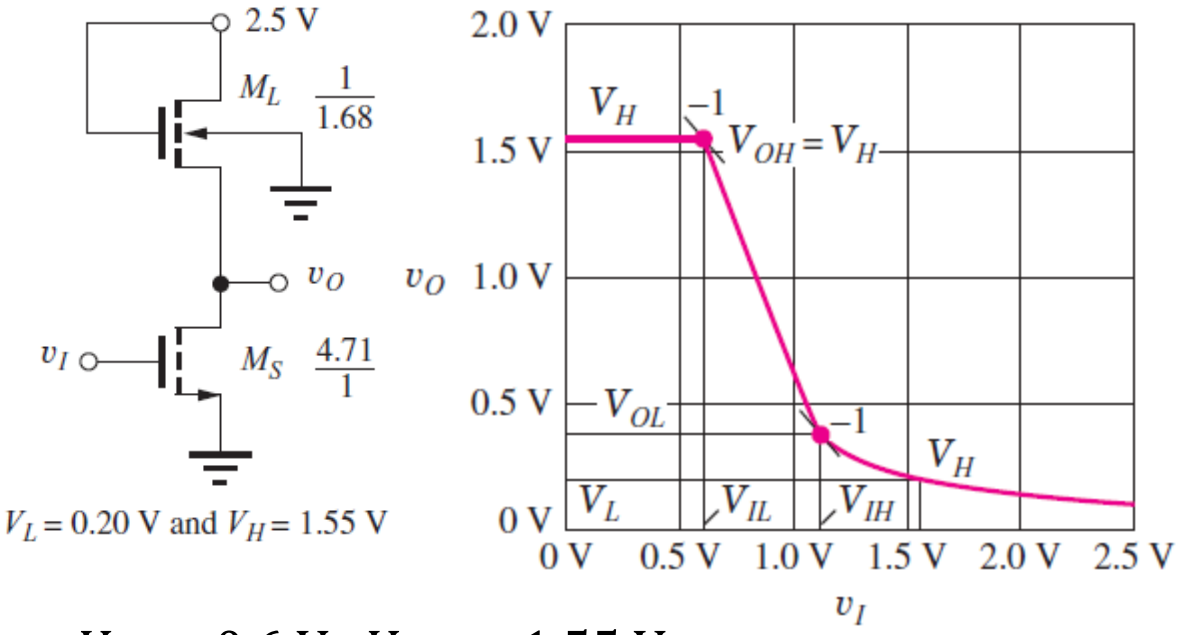


$v_I = V_H, v_O = V_L$

$v_I = V_H$, M_S triode, M_L saturation

- Use the same conditions as before:
  $I_{DD} = 80\ \mu\text{A}, V_L = 0.20\ \text{V}$
- Except $V_H = 1.55\ \text{V} \neq V_{DD}$!
- Triode region equation for M_S:
  $$i_D = K_n'\left(\frac{W}{L}\right)_S\left(v_{GS} - V_{TNS} - \frac{v_{DS}}{2}\right)v_{DS}$$
- $v_{GS} = V_H = 1.55\ \text{V}, v_{DS} = V_L = 0.2\ \text{V}, V_{TNS} = 0.6\ \text{V} \Rightarrow \left(\frac{W}{L}\right)_S = \frac{4.71}{1}$

Noise margin analysis



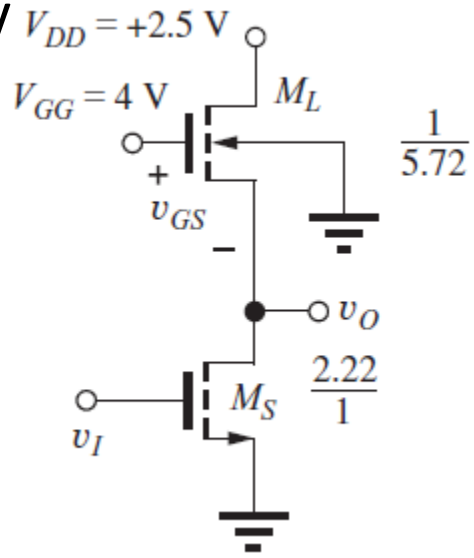
Completed inverter design and SPICE simulation of VTC for NMOS inverter with saturated load

- $V_{IL} = 0.6$ V, $V_{OH} = 1.55$ V
- $V_{IH} = 1.12$ V, $V_{OL} = 0.38$ V
- $\mathrm{NM}_H = 0.43$ V, $\mathrm{NM}_L = 0.22$ V
- NM_H is significantly reduced, NM_L is similar

NMOS linear load inverter

K_n'=100μA/V²

V_{TO}=0.6 V



Choose V_{GG} such that $V_{GG} > V_{DD} + V_{TNL}$

M_L: Always in triode region

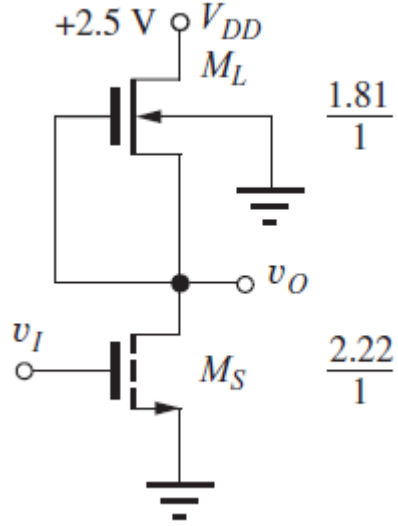
- For M_L:

$v_{GS} - V_{TNL} = V_{GG} - v_O - V_{TNL} \geq V_{DD} + V_{TNL} - v_O - V_{TNL} = V_{DD} - v_O = V_{DS} \Rightarrow$ Always in triode (linear) region.

- Body effect exists for M_L
  - $v_{SB} \neq 0$ for M_L ! In fact, $v_{SB} = v_O$

NMOS depletion-mode load inverter

K_n'=100μA/V²
V_{TO}=-1 V

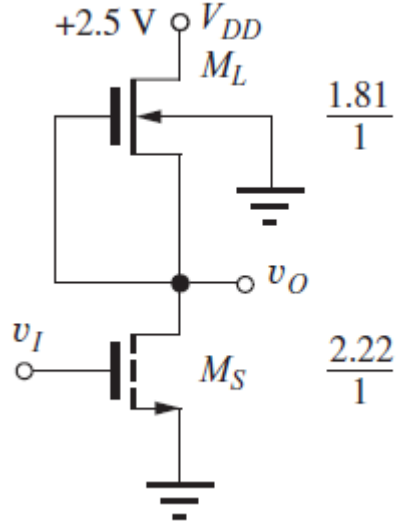


For M_L: $v_{GS} = 0, V_{TN} < 0$
⇒ Always on
(designed to be saturated)

- $v_I = V_L$, M_S is off, M_L conducts current until $v_{DS} = 0$ ($v_O = V_{DD}$), thus $V_H = V_{DD}$
- $v_I = V_H, v_O = V_L$, for M_L
  - $v_{GS} - V_{TNL} = -V_{TNL}$
  - $v_{DS} = v_{DD} - v_O$
  - As long as $v_{DD} - v_O > -V_{TNL}$, M_L in saturation
- Body effect exists for M_L
  - $v_{SB} \neq 0$ for M_L ! In fact, $v_{SB} = v_O$

Design of $\left(\frac{W}{L}\right)_S$ and $\left(\frac{W}{L}\right)_L$

K_n'=100μA/V²
V_{TO}=-1 V



For M_L: $v_{GS} = 0, V_{TN} < 0$
⇒ Always on
(designed to be saturated)

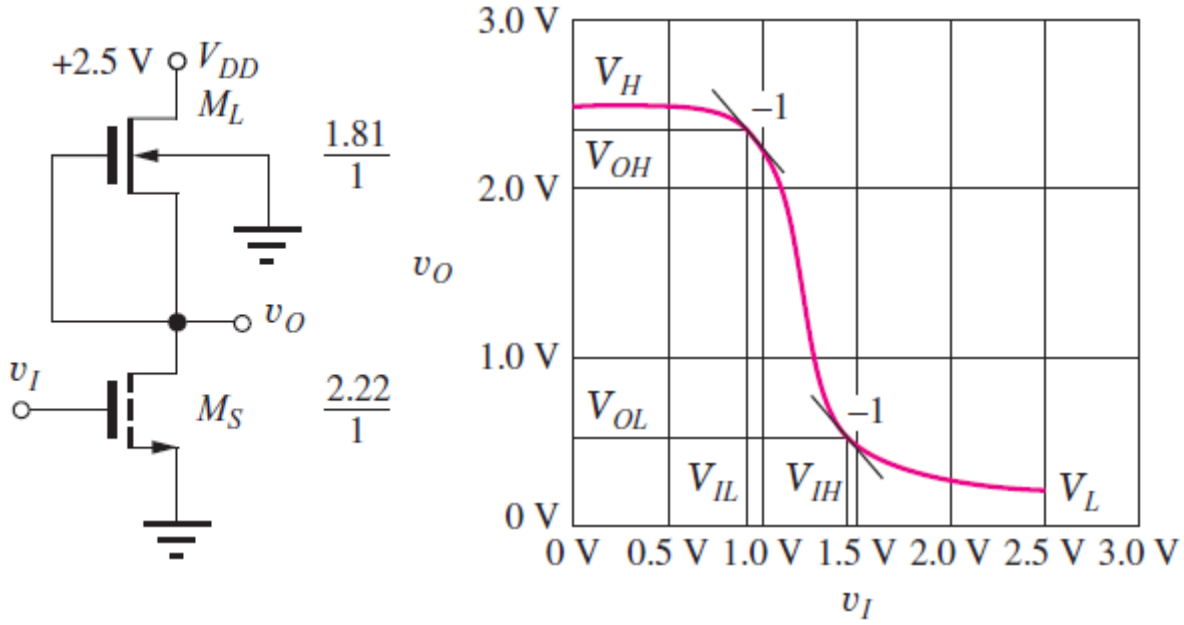
$v_I = V_H$, M_S triode, M_L saturation

- $I_{DD} = 80\mu\text{A}, V_L = 0.20\text{V}, V_H = 2.5\text{V}$
- Saturation region equation for M_L:

$$i_D = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (0 - V_{TNL})^2$$

- Body effect for M_L:
- $V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_L + 2\phi_F} - \sqrt{2\phi_F}\right) = -0.94\text{ V}$
- This gives $\left(\frac{W}{L}\right)_L = \frac{1.81}{1}$
- For MS, the same as in the resistive load case, thus $\left(\frac{W}{L}\right)_S = \frac{2.22}{1}$

Noise margin analysis

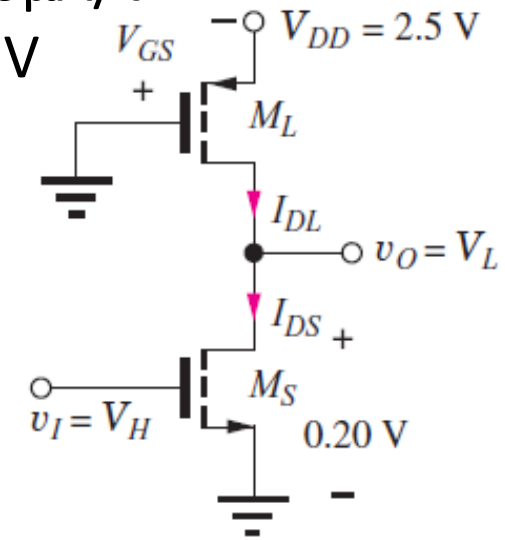


Completed inverter design and SPICE simulation of VTC for NMOS inverter with depletion-mode load

- $V_{IL} = 0.93\ \text{V},\ V_{OH} = 2.35\ \text{V}$
- $V_{IH} = 1.45\ \text{V},\ V_{OL} = 0.50\ \text{V}$
- $\text{NM}_H = 0.90\ \text{V}, \text{NM}_L = 0.43\ \text{V}$
- NM_H is high as in resistive load, NM_L is improved

Pseudo NMOS inverter

K_n'=100μA/V²
V_{TO}=-1 V



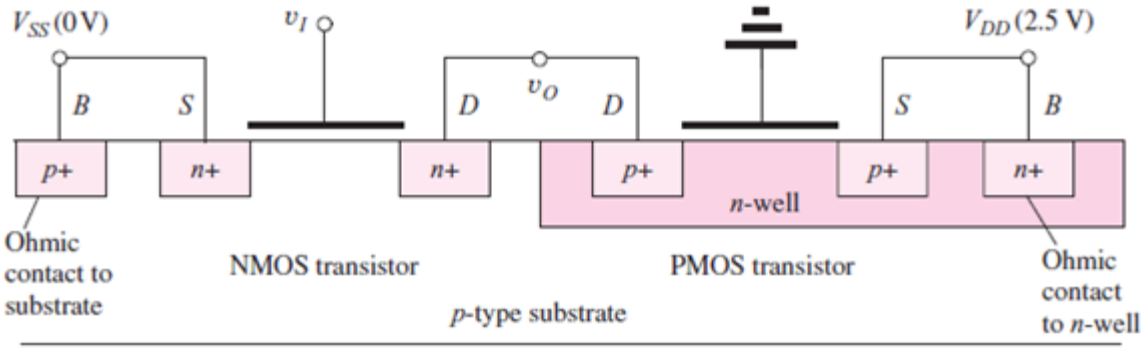
- For M_L:

$V_{GS} < V_{TNL} \Rightarrow$ On

When $v_O = V_L$, $|V_{DS}| < |V_{GS} - V_{TN}| \Rightarrow$ saturated

$V_H = V_{DD} \Rightarrow$ no degradation of V_H

- No body effect for M_L !
  - Bulk and source are connected for M_L



NMOS Inverter Comparison

	Pros	Cons
Resistive Load	Simple	Takes too much area
Saturated Load	Simple	Degradation of V_H Poor speed
Linear Load	faster speed	Additional power supply
Depletion-mode load	Saves area Best Noise Margin High speed	Process complexity (Implant)
Pseudo NMOS	Smallest area Best speed	Process complexity (PMOS, Implant)